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Objectives:

The objective for this week will be understanding the designing of basic sequential circuits along with finite state machines

- Mealy State Machines

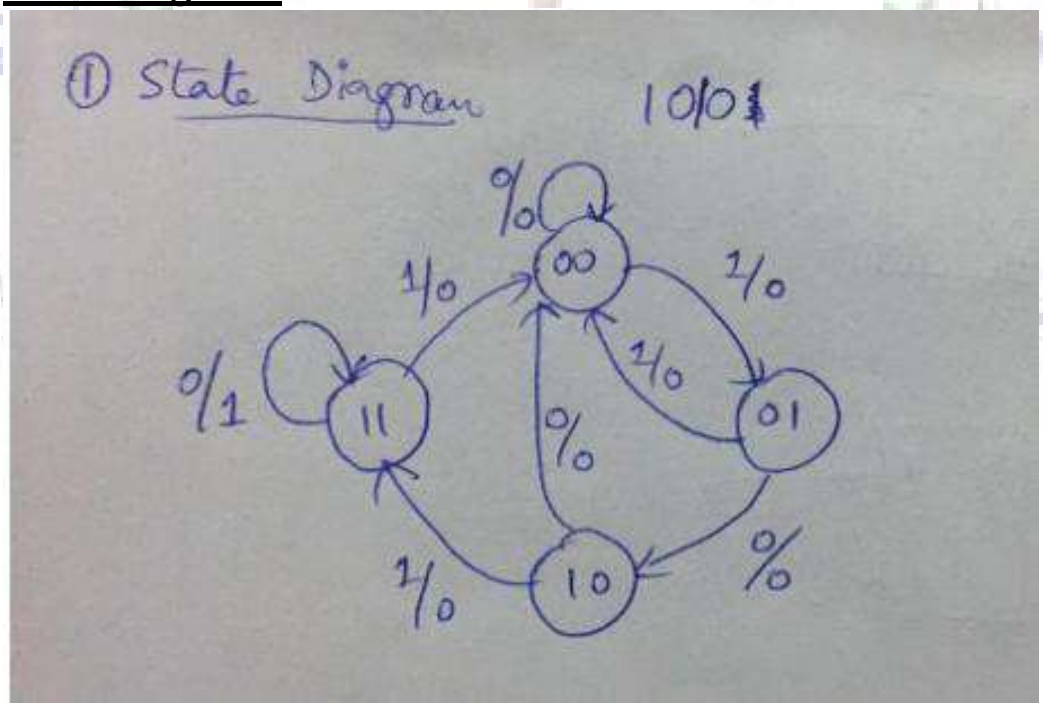
LECTURE-29-30

:Mealy State Machines:

Example#1:

Design a password based lock using mealy state machine, the password to be used will be 1010.

- **State Diagram:**



- **State Table:**

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② State Table

Input x	Current States Q_1	Q_2	Next States Q_1	Q_2	Flip Flop Inputs D_1	D_2	Output lock (Z)
0	0	0	0	0	0	0	0
1	0	0	0	1	0	1	0
0	0	1	1	0	1	0	0
1	0	1	0	0	0	0	0
0	1	0	0	0	0	0	0
1	1	0	1	1	1	1	0
0	1	1	1	1	1	1	1
1	1	1	0	0	0	0	0

- **Flip Flop Input Equations and Output lock Equation:**

Digital Logic Design (ESC-151)

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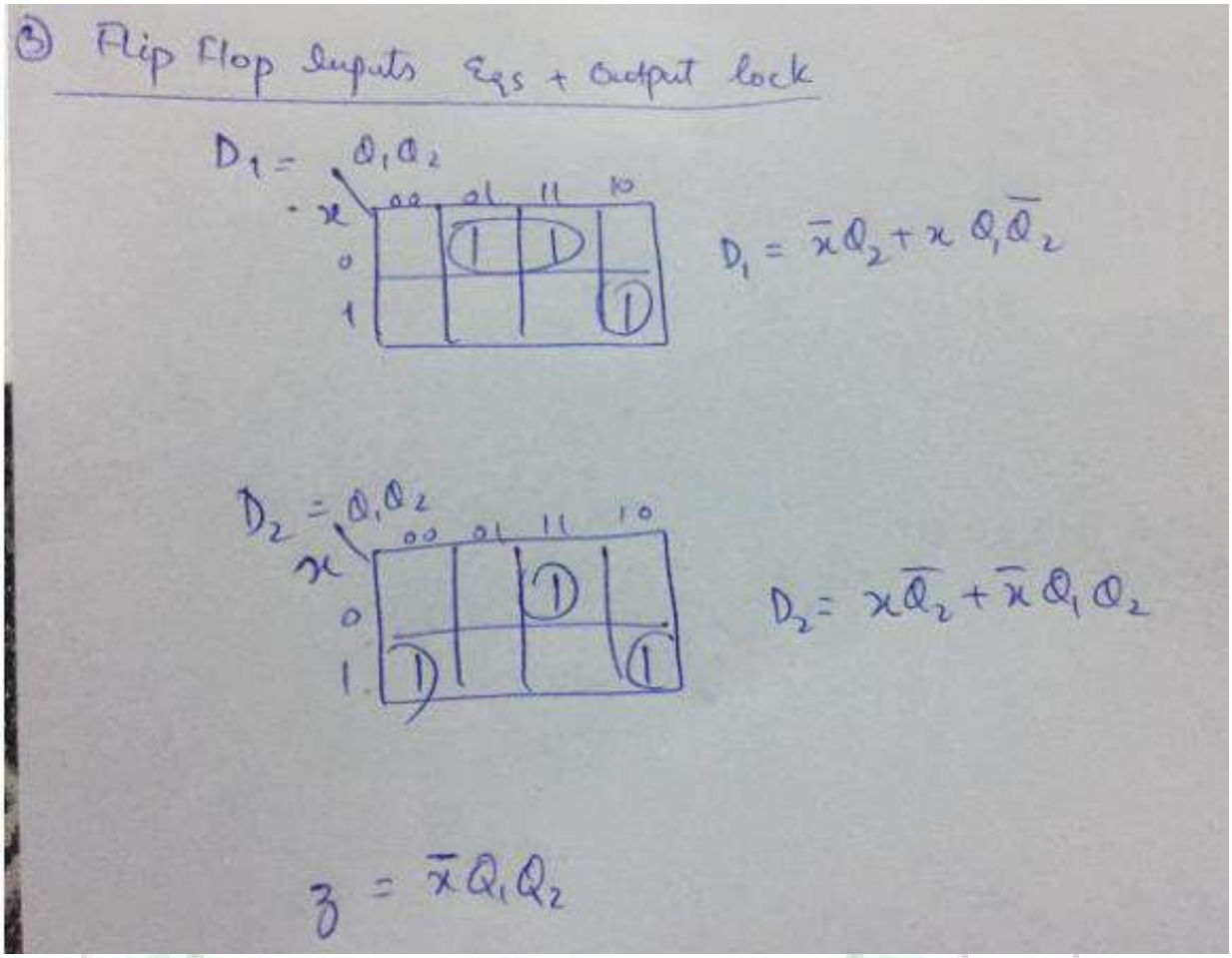

- **Circuit Diagram:**

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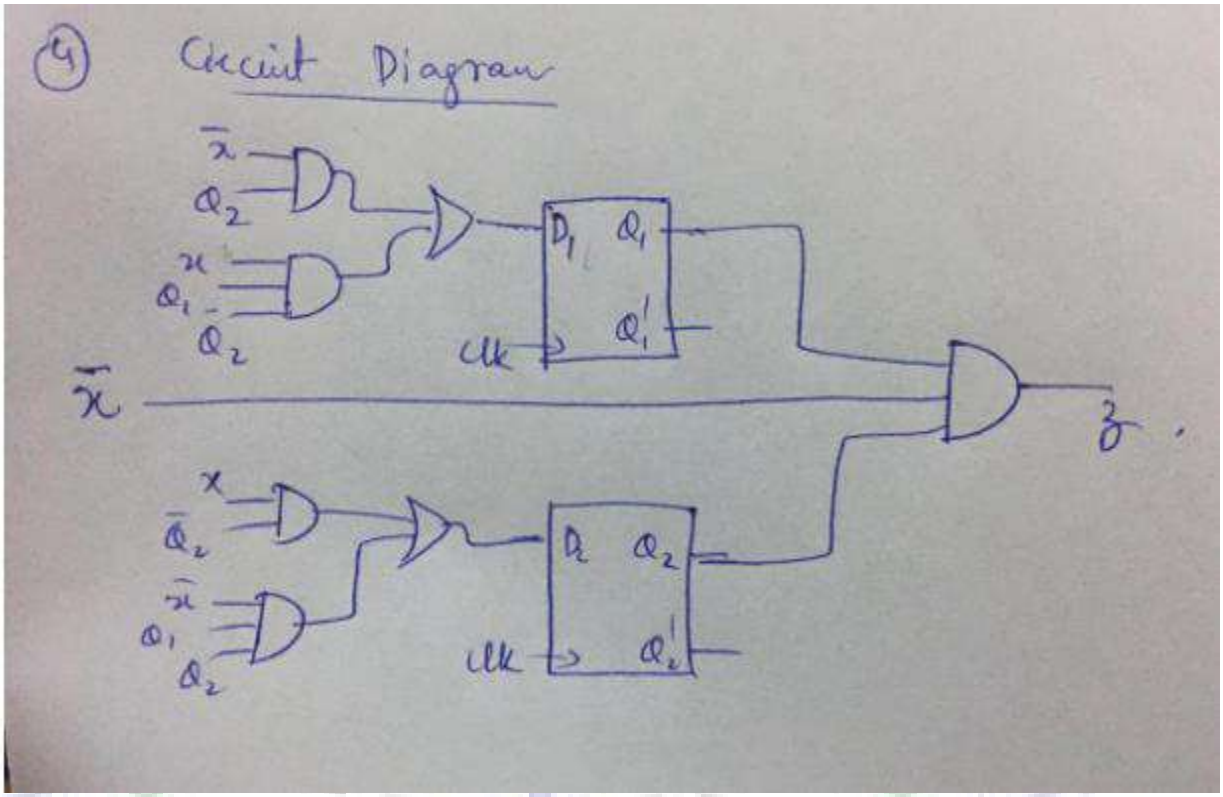
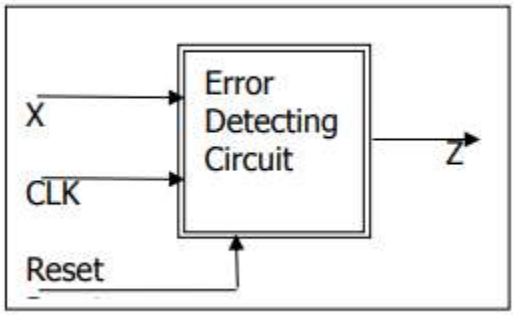


Example#2:

Design an error detector for the following sequential circuit. The circuit has a single input x and a single output z. Data arrive serially on x synchronized with the clock. The output z (an error) should be "1" whenever two consecutive zeroes or three consecutive ones appear on line x.



- **State diagram:**

Digital Logic Design (ESC-151)

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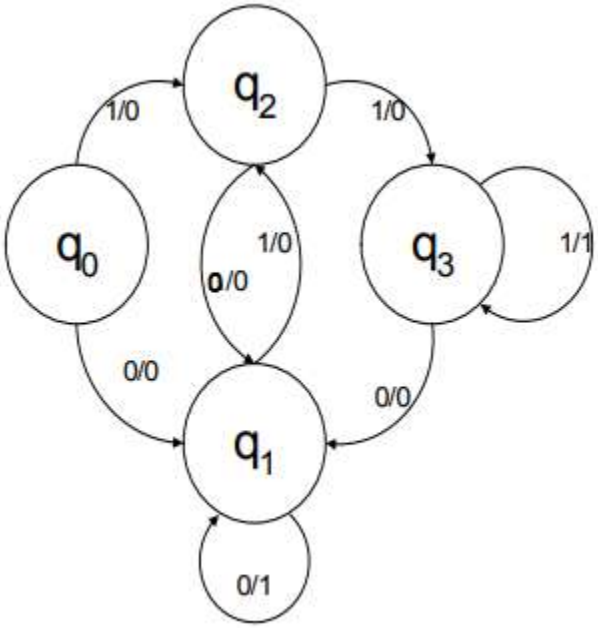

- **State assignment:**
  q0=00 q1=01 q2=10 q3=11
- **State Table:**

Input x	Current states y1y0	Next states y1y0	Flip flop inputs D1D0	Output error
0	00	01	01	0
1	00	10	10	0
0	01	01	01	1
1	01	10	10	0
0	10	01	01	0
1	10	11	11	0
0	11	01	01	0
1	11	11	11	1

- **Flip flop input equations and output equations:**

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y_1 y_0 \ x	0	1
00	0	1
01	0	1
11	0	1
10	0	1

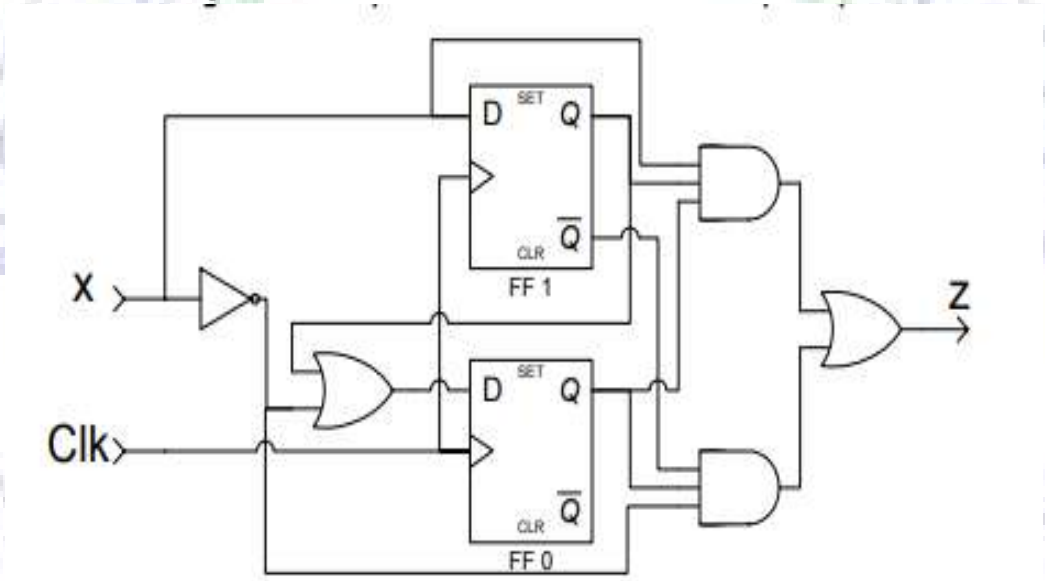
$$y_1^+ = D_1 = x$$

y_1 y_0 \ x	0	1
00	1	0
01	1	0
11	1	1
10	1	1

$$y_0^+ = D_0 = \bar{x} + y$$

$$\text{error} = z = \bar{y}_1 y_0 \bar{x} + y_1 y_0 x$$

- **Circuit diagram:**



Example#3:

Draw state table for following mealy state diagram:

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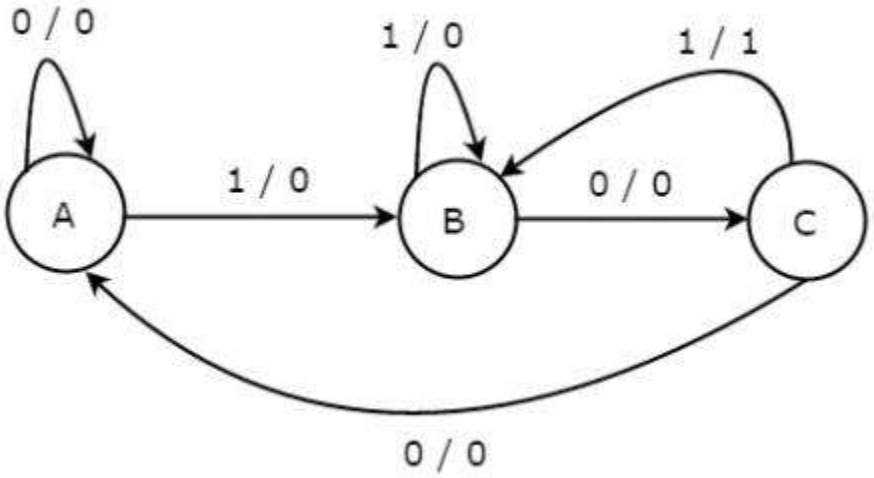

State Table:

input	Current states	Next states	Flip flop inputs	output
0	A	A	A	0
1	A	B	B	0
0	B	C	C	0
1	B	B	B	0
0	C	A	A	0
1	C	B	B	1

Example#4:

Draw mealy state diagram for following state table:

input	Current states	Next states	Flip flop inputs	output
0	Q0	Q1	Q1	0
1	Q0	Q2	Q2	0
0	Q1	Q1	Q1	0
1	Q1	Q2	Q2	1
0	Q2	Q1	Q1	1
1	Q2	Q2	Q2	0

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- **State diagram:**