Computer Architecture ECS-355

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(Week 10) Lecture 19-20

Learning objectives:

- Review of the last lecture
- General Register Organization
- Control Word and example of Microoperations

(Note: It is important to note that we are considering "Basic computer architecture" processor which we were discussing in the class and it's the continuation of the same concepts. Another important point is that brief part of the last lecture is repeated. Audio clip will be sent separately for every diagram.)

Resources: Beside these lecture handouts, this lesson will draw from the following

Text Book: Computer System Architecture by Morris Mano (3rd Edition) and **Reference book:Computer Architecture, by William Stallings (4th Edition)**.

Lecture:

Introduction

The part of the computer that performs the bulk of data processing operations is called the **central processing unit** and is referred to as the CPU. The CPU is made up of three major parts, as shown in Fig. 1. The **register set** stores intermediate data used during the execution of the instructions. The **arithmetic logic unit (ALU)** performs the required microoperations for executing the instructions. The **control unit** supervises the transfer of information among the registers and instructs the ALU as to which operation to perform. The CPU performs a variety of functions dictated by the type of instructions that are incorporated in the computer.

Computer architecture is sometimes defined as the computer structure and behavior as seen by the programmer that uses machine language instructions. This includes the instruction formats, addressing modes, the instruction set, and the general organization of the CPU registers. One boundary where the computer designer and the computer programmer see the same machine is

the part of the CPU associated with the **instruction set**. From the designer's point of view, the computer instruction set provides the specifications for the design of the CPU. The design of a CPU is a task that in large part involves choosing the hardware for implementing the machine instructions. The user who programs the computer in machine or assembly language must be aware of the register set, the memory structure, the type of data supported by the instructions, and the function that each instruction performs.

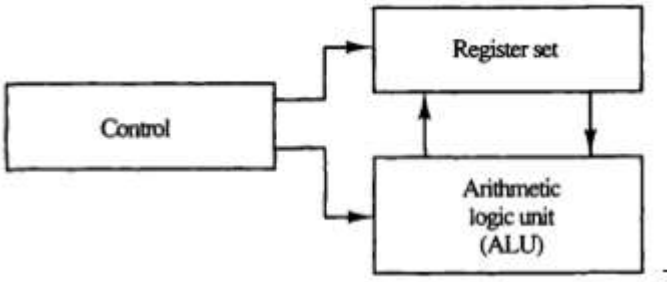

Figure.1 Major Components of CPU

CPU has following components as

1. Storage Components
    a. Registers
    b. Flags
2. Execution Components
    a. ALU
3. Transfer Components
    a. Addresss Bus
    b. Control Bus
    c. Data Bus
4. Control Components
    a. Control Unit

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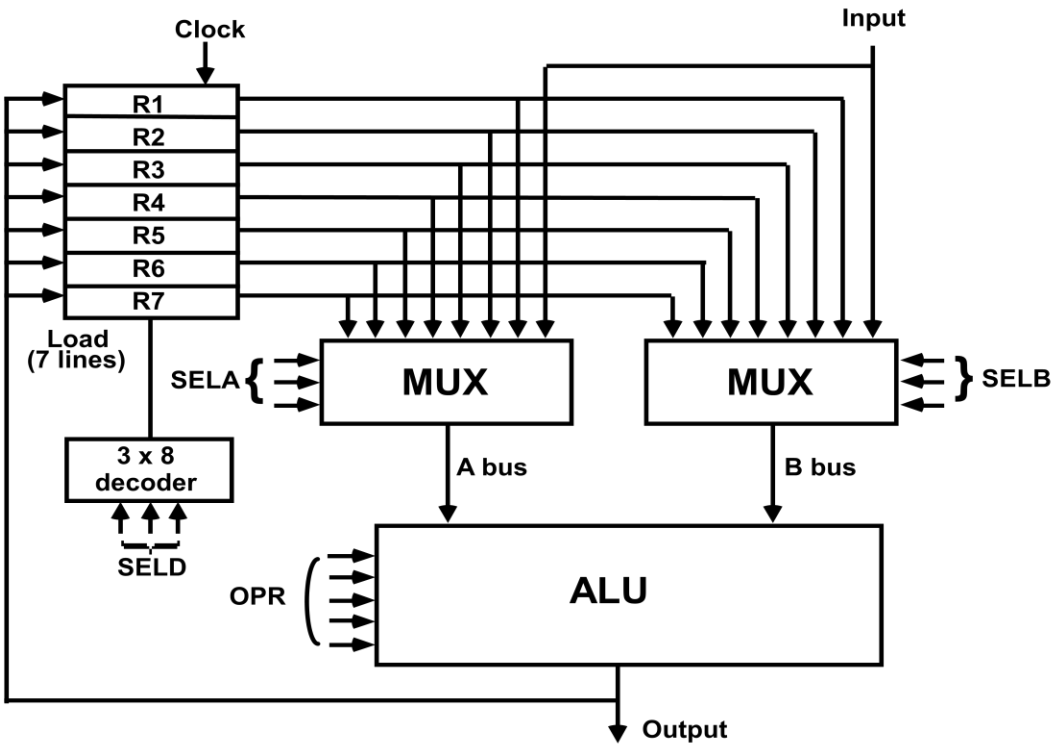
General Register Organization

In this organization there are arbitrary number of registers in the CPU that can be used interchangeably. In the following diagram there are seven registers named R1.. R7, that can be selected using a 3x8 decoder with selection lines named SEL-D for sake of storing the result of ALU.

The output of any of these registers (Operands) along with the input can be forwarded to the ALU by two multiplexers. MUX-A will forward the first operand while MUX-B will forward the second operand by means of selections lines SEL-A and SEL-B respectively. Similarly the OPR selection will select the possible operation being performed by ALU.

Note that the 000 combination of SEL-A and SEL-B will forward possible inputs while in case of SEL-D the result will be sent for output directly.



Operations of Control Unit

The control unit directs the information flow through ALU by

- Selecting various *Components* in the system

- Selecting the *Function* of ALU

Example:

R1 ← R2 + R3

- MUX A selector (SELA): BUS A ← R2
- MUX B selector (SELB): BUS B ← R3
- ALU operation selector (OPR): ALU to ADD
- Decoder destination selector (SELD): R1 ← Out Bus

Control Word

There are 14 binary selection inputs in the unit, and their combined value specifies a control word. The 14-bit control word is defined in Fig.2. It consists of four fields. Three fields contain three bits each, and one field has five bits. The three bits of SELA select a source register for the A input of the ALU. The three bits of SELB select a register for the B input of the ALU. The three bits of SELD select a destination register using the decoder and its seven load outputs. The five bits of OPR select one of the operations in the ALU. The 14-bit control word when applied to the selection inputs specify a particular microoperation.

Figure.2 Control word

Encoding of Register selection field

Binary Code	SELA	SELB	SELD
000	Input	Input	None
001	R1	R1	R1
010	R2	R2	R2
011	R3	R3	R3
100	R4	R4	R4
101	R5	R5	R5
110	R6	R6	R6
111	R7	R7	R7

ALU Control

The ALU provides arithmetic and logic operations. In addition, the CPU must provide shift operations. The shifter may be placed in the input of the ALU to provide a pre-shift capability, or at the output of the ALU to provide post-shifting capability.

Encoding of ALU Operations

OPR Select	Operation	Symbol
00000	Transfer *A*	TSFA
00001	Increment *A*	INCA
00010	Add *A* + *B*	ADD
00101	Subtract *A* − *B*	SUB
00110	Decrement *A*	DECA
01000	AND *A* and *B*	AND
01010	OR *A* and *B*	OR
01100	XOR *A* and *B*	XOR
01110	Complement *A*	COMA
10000	Shift right *A*	SHRA
11000	Shift left *A*	SHLA

Example of ALU microoperations

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Symbolic Designation					
Microoperation	SELA	SELB	SELD	OPR	Control Word
R1 ← R2 - R3	R2	R3	R1	SUB	010 011 001 00101
R4 ← R4 ∨ R5	R4	R5	R4	OR	100 101 100 01010
R6 ← R6 + 1	R6	-	R6	INCA	110 000 110 00001
R7 ← R1	R1	-	R7	TSFA	001 000 111 00000
Output ← R2	R2	-	None	TSFA	010 000 000 00000
Output ← Input	Input	-	None	TSFA	000 000 000 00000
R4 ← shl R4	R4	-	R4	SHLA	100 000 100 11000
R5 ← 0	R5	R5	R5	XOR	101 101 101 01100